A Glimpse at Long-term Effects of Momentary Overvoltages on Zinc Oxide Varistors

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Significance:
Part 6 - Textbook, tutorials and reviews

A brief paper presented to the community of ceramics researchers on the same theme as the Zurich EMC 1989 Symposium paper by the same authors on the long range effects of swells and alerting them to the pitfalls of selecting excessively low clamping voltages in the misguided perception that the protective function would be improved. The theme is supported by a theoretical modeling of the overheating of the ceramic material that could eventually result in thermal runaway (see “Selecting Varistor Clamping Voltage: Lower is not Better!” in Part 7). That concern led to the experimental work reported in “The Effect of Repetitive Swells on Metal-Oxide Varistors” in 1992, also available in Part 7 of this Anthology

A GLIMPSE AT LONG-TERM EFFECTS OF MOMENTARY OVERVOLTAGES ON ZINC OXIDE VARISTORS

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ABSTRACT

Because the prime function of varistors is the diversion of high energy surges, most of the attention is directed toward selecting the appropriate device rating to ensure long life under surge conditions. Some attention is also given to matching steady-state rating of the device to the power system voltage. However, during abnormal (and not well defined) power system conditions, the line voltage can reach values that will cause substantial current in the varistor. Until the effects of these momentary overvoltages are better identified and understood, there will be a risk of near-term failure at worst and accelerated aging at best.

SELECTION OF VARISTOR RATINGS

Selection of a varistor rating is essentially a process of matching the capabilities of the device to the power system environment, while obtaining the desired low clamping voltage during surge events. Low clamping voltage of a varistor may be obtained in one of two ways, or both: low current density at the surge current, which means a relatively large area, or low intrinsic voltage, which means a relatively thin disc. Increasing the area of a disc increases the device cost so that the natural tendency of designers will be to seek the thinner disc rather that the larger diameter disc. Therefore, this paper addresses the concerns raised by excessive reduction of disc thickness, that is, the use of varistors with rated line voltage lower than what prudent practice would indicate.

In matching a varistor to its environment, the two principal environment characteristics to be considered are: (1) the surges expected to occur on the system -- the primary reason for using the varistor -- and (2) the system rated voltage. In the application of surge arresters to electric utility systems, considerable attention is given to abnormal power system conditions, as evident in the rating of these arresters which takes into consideration the maximum continuous operating voltage (MCOV) permissible for an arrester.[1]

In the the case of low-voltage electronic circuits, equipment designers generally rely on the manufacturer's rating of a device for the stated nominal system voltage. This system voltage is defined with some expected tolerance, such as 15%, on the maximum voltage that can occur.

Surge ratings - Specification sheets published by varistor manufacturers generally include a "Pulse Rating" family of curves showing the number of permissible surges (pulses) as a function of current amplitude and duration. This pulse rating makes it possible to select a device of appropriate dimensions -- that is, current handling capability -- to ensure survival in the known or postulated surge environment [2]. Actually, survival means more than the non-occurrence of a catastrophic failure. For varistors used in electronic equipment, the criterion for end of life, or total consumption of the Pulse Rating, is a change of more than 10% in the device nominal voltage. The actual process leading to this change in device characteristic is not clearly described by the manufacturers literature, but is generally believed to involve microscopic damage to the structure.

Steady-state vs. momentary ratings - The steady-state rating is generally determined by the manufacturers, on the basis of in-house experience. This process is reflected in the wording of an IEEE Standard on varistors defining "Rated RMS Voltage" as follows: *There is no single test that can determine the voltage rating, but rather an evaluation process taking into consideration .... These considerations are within the realm of the manufacturer's and user's application engineering functions.* [3] In plain English, this means that there is no clear-cut guidance available; rather, designers are left on their own to make the hard choices. The manufacturers, however, do publish an Arrhenius plot of mean life versus temperature, implying high activation energy levels in the processes leading to the end of life under steady-state line voltage.

Field experience has shown that the expectation of a + 15% maximum deviation of line voltage is optimistic. The term "swell" has been proposed [4] to describe the occurrence of a momentary increase of the sinusoidal line voltage amplitude, lasting from a few cycles to a few seconds. During such a swell, the normal standby current of the varistor will increase in accordance with the varistor power law. For instance, a 20% increase in line voltage (a factor of 1.2) rather than the 15% often considered as the "high-line limit" by designers, with a varistor exponent of 32, produces an increase of the standby current of 1.2 elevated to the 32th power -- a 340-fold increase ! This current level can no longer be considered a benign "standby current."

Thus, the selection process of a varistor must also include proper attention to the long-term effects of repeated swells. A search of the literature reveals that no work has been published on these effects.

Perhaps one of the reasons for this lack of information is that very little specific information has been collected on the severity of swells occurring in power systems. The electric utilities and their customers have recently increased their awareness of the so-called *Power Quality* issue, as a result of concerns over the performance of increasingly sophisticated electronic equipment supplied by a disturbance-prone power system. One of the effects of these concerns has been the development of disturbance monitors with graphics capability. As more and more of these monitors are applied, the occurrence and characteristics of swells will become much better known.

Thus, between the well-defined bounds of short-time surges and the less defined steady-state voltage rating, neither the occurrence nor the effects of repeated swells are well defined. Faced with this lack of information, the authors have initiated a joint project of experimental and theoretical evaluation of the effect of repeated swells on zinc oxide varistors. The experimental work consists essentially in applying repeated swells of various amplitudes and durations, seeking to detect some change in the electrical characteristics of the varistor that would herald the onset of objectionable degradation. The theoretical work consists in modeling the behavior of the varistor, essentially its temperature, in response to a variety of swells. To fully understand the science involved, however, this work should be complemented by fundamental studies on the degradation mechanisms leading to any observed change in the electrical characteristics. One of the purposes of this paper is to motivate ceramists toward looking into the effects of swells from the point of view of ceramic structural changes. In the meantime, the experimental work, supported by modeling to identify the impact of various levels of swells, will draw the attention of equipment designers to the pitfalls of selecting excessively thin discs.[5]

MODELING THE EFFECT OF SWELLS

A circuit analysis model of a metal-oxide varistor was used to investigate the behavior of varistors when exposed to swells . The model consists of two parts: The electrical part of the model predicts the current-voltage behavior of the varistor and the thermal part of the model predicts the temperature changes caused by the energy deposited in the varistor during the swell. The electrical and thermal simulations were performed using a commercial software system which uses behavioral equations to mimic nearly any physical device or process.

The model computations were performed for a varistor rated at 130 V rms. Such a varistor is the lowest rating offered by manufacturers for a 120 V circuit. To represent a possible worst case, the varistor characteristics used for the model computations were set at the lower limit of the tolerance band. To simplify the model, no allowance is made for heat loss by convection, the situation that can be expected in a tight packaging without any encapsulation. Heat losses by radiation are negligible at the temperatures involved. These postulates provide worst case results, a justifiable approach when considering reliability.

Figure 1 shows an example of the output plot of the model computations, for a 206 V peak line voltage (145 V rms, a 20% swell). The current exhibits the highly nonlinear response of a varistor, with 20 mA peaks. The resulting temperature increase steps are also plotted for each successive pulse, occurring at the 120 pulse-per-second rate. As the temperature increases, so will heat losses, until a thermal equilibrium is reached, unless thermal runaway would occur.

Figure 2 shows the temperature rise predicted for the application of swells at two voltage levels beyond the 20% swell of Figure 1, each with a duration of 200 s. This 200 s duration was selected because it approximates the time required to reach thermal equilibrium in this model, not because of an inference that power system swells last 200 s. The lower curve shows the temperature rise of approximately 130 °C expected from 156 V rms (a 30% swell). The upper curve shows a temperature rise of nearly 300 °C for 160 V rms (a 33% swell). These curves illustrate that a relatively small change in the swell level, from 156 V to 160 V rms, produces a drastic increase in the power dissipation and the temperature rise of a varistor. The 300 °C temperature rise means assured destruction of the varistor, the 130 °C temperature could mean some accelerated aging, if repeated enough times. Thus, the cumulative effect of repeated swells needs to be evaluated. This evaluation is the subject of the experimental work.

EXPERIMENTS WITH REPEATED SWELLS

Several factors are known or suspected in the behavior of actual varistors exposed to repeated stress, complicating the apparent simplicity of varistor modeling. Aging -- a change in the varistor characteristics in response to overstresses -- is only one of them. Even when considering only aging, there is no universally recognized criterion of degradation. Most varistor specifications refer to a 10% limit in changes of the nominal voltage of the varistor. However, since this nominal voltage is defined arbitrarily for a 1 mA current regardless of the varistor cross section, the criterion varies with varistor sizes. Another proposed criterion, power dissipation at some ac voltage, is complicated by the fact that the power dissipation changes with the duration of application of the steady-state as well as swell ac voltages.

This effect, which permanently changes the characteristics of the varistor, sometimes called "formation," was quite apparent when successive swells were applied. During application of one swell, for instance, the increasing temperature of the varistor is reflected in the increased peak amplitude of the current, as shown in Figure 3A. However, when comparing the pattern of current peaks within the first swell to the pattern of a later swell, after many additional swells (Figure 3B), the most obvious change is a reduction of the current peaks between the original swell and the later swell. Thus, a systematic method to account for that "formation" effect must be developed to define a valid criterion of aging before conclusions can be drawn on quantifying the aging effect of swells.

CONCLUSIONS

Attempts at improving surge protection by selecting varistors with low voltage ratings increase the risk of premature aging, even early failure, of varistors exposed to repeated momentary overvoltages ("swells").

The effects of such repeated swells have not been documented by the manufacturers, although it is a subject of investigation that would provide useful results for greater reliability. Additional theoretical and experimental work is necessary to develop guidance useful to prudent equipment designers.

While the occurrence of these swells has not been well characterized in the past, the increasing availability of power line disturbance monitors will improve this characterization in the future. Combined with a better understanding of the effects of swells, this knowledge will enhance the reliable application of metal-oxide varistors.

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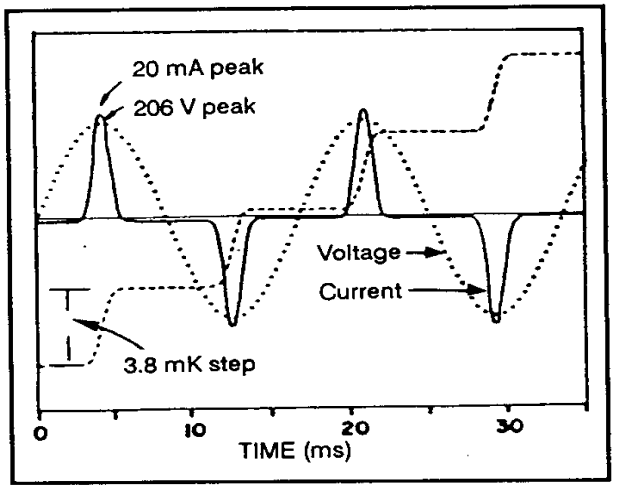

Figure 1. Computed instantaneous temperature increase of a varistor during two cycles of a 20% swell

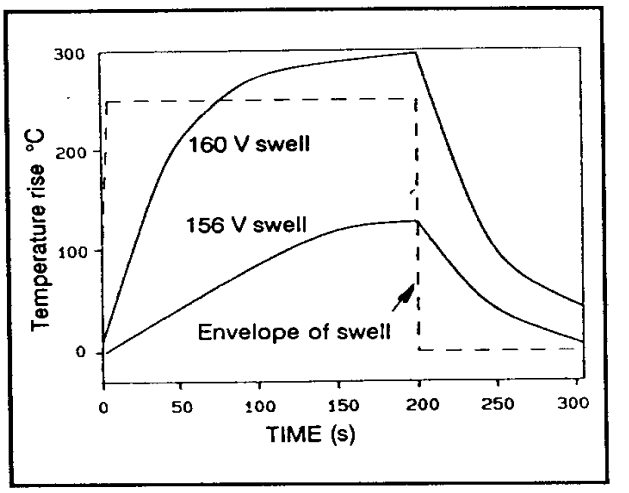

Figure 2. Computed integrated temperature increases during a 30% swell and a 33% swell

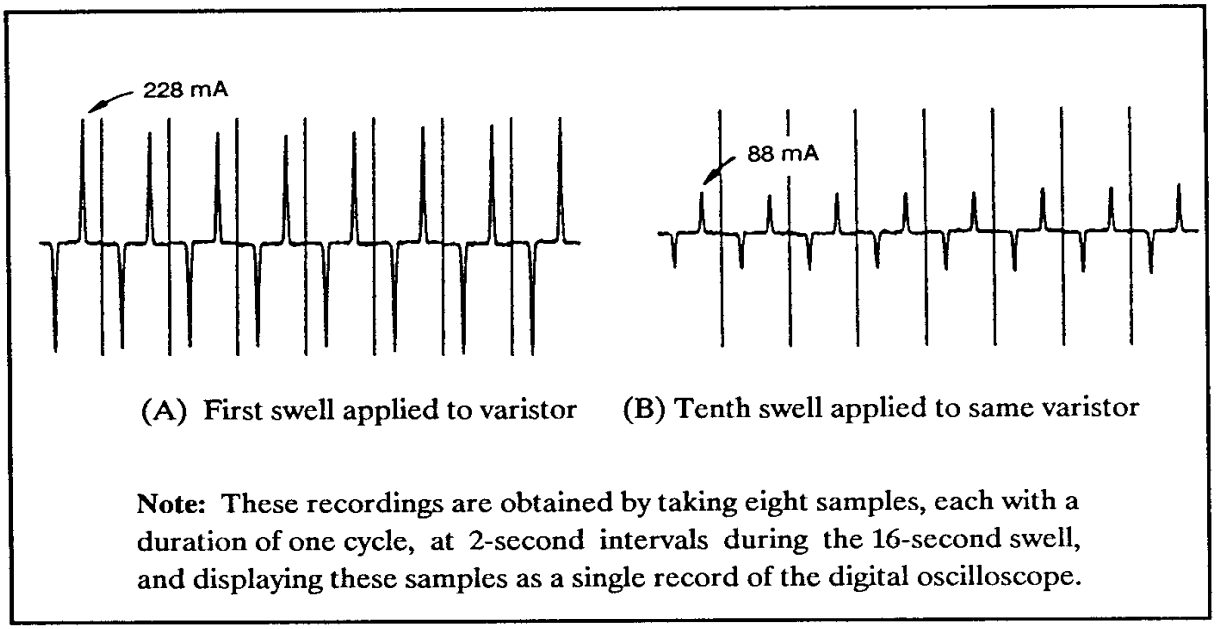

Figure 3. Samples of varistor current during a 16-second swell with peak voltage at 117% of the varistor nominal voltage